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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/032,734	12/28/2001	Salman Akram	2754.4US (95-0742.4)	6382

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	**PAPER NUMBER**
2822	

DATE MAILED: 04/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/032,734	AKRAM ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-7,11-21,23-25 and 29-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-7,11-21,23-25 and 29-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1 page*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2, 4-7, 11-21, 23-25 and 29-36 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Corbett (4992850).

At column 2, lines 45-46; column 3, lines 3-8; column 3, line 59 to column 4, line 3; column 4, lines 31-33; column 5, lines 1-44; column 5, lines 61-65; column 6, lines 1-2, 10-18; column 6, line 45 to column 7, line 4; column 7, lines 22-42 and 56-66; and column 8, lines 15-59, Corbett discloses the following:

A multi-chip module system comprising: a substrate 23 having at least a first position having, in turn, a predetermined configuration 25 for locating a first semiconductor device thereat and having at least one other vacant position having, in turn, a predetermined configuration 25 for locating a second semiconductor device (any one of the devices 31) thereat on the multi-chip module system, the at least one other vacant position

having no semiconductor device located thereat; and a first semiconductor device (any one of the devices 31 other than the first device) located in the at least first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic (the performance characteristic of being not defective); said first semiconductor device has been burned in; the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat which is substantially the same as the predetermined configuration of the first position; the at least one other vacant position having the predetermined configuration for locating the second semiconductor device thereat; and the second semiconductor device having a second predetermined performance characteristic at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device.

A multi-chip module system comprising: a substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration 25 for locating a second semiconductor device thereat, and having at least one other vacant position having, in turn, a predetermined configuration for locating a third semiconductor device (any

one of the devices 31 other than the first or second device) thereat on the multi-chip module system, the at least one other vacant position having no semiconductor device located thereat; the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and the second semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; said first and second semiconductor devices have been burned in; the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat which is substantially the same as the predetermined configuration of the first position; the at least one other vacant position having a predetermined configuration for locating a third semiconductor device thereat; and the third semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device; wherein the first semiconductor device comprises a memory device; wherein the second semiconductor device comprises a memory device; wherein the first semiconductor device comprises a microprocessor device; wherein the

second semiconductor device comprises a microprocessor device; wherein the multi-chip module system comprises a single in-line memory module system; a third semiconductor device; 31 and an adapter "a circuit compatible with the existing circuit" connected to the third semiconductor device, the adapter having a configuration for connecting the adapter to the at least one other vacant position on the substrate to allow connection of the third semiconductor device to the substrate.

A multi-chip module system comprising: a substrate having two opposing sides, said substrate having a first position having, in turn, a predetermined configuration for locating a first semiconductor device thereat, having a second position having, in turn, a predetermined configuration for locating a second semiconductor device thereat, having a first vacant position having, in turn, a predetermined configuration for locating a third semiconductor device thereat, the first vacant position having no semiconductor device thereat; and having a second vacant position having, in turn, a predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system; the second vacant position having no semiconductor device located thereat; the first semiconductor device located in the first position of the substrate for use in the multi-chip module system, the first semiconductor device having a first

predetermined performance characteristic; and the second semiconductor device located in the second position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; said first and second semiconductor devices being burned in; the first vacant position and the second vacant position are on opposing sides of the substrate.

A multi-chip module system comprising: a substrate having at least a first predetermined configuration position for locating a first semiconductor device thereat and having at least one other vacant predetermined configuration position for locating a second semiconductor device thereat on the multi-chip module system; and the first semiconductor device located in the at least the first predetermined configuration position of the substrate for use in the multi-chip module system, the at least one other vacant position having no semiconductor device located thereat, the first semiconductor device having a first predetermined performance characteristic; said first semiconductor device being burned in; the at least one other vacant predetermined configuration position for locating the second semiconductor device thereat which is substantially the same as the predetermined configuration of the first position; the at least one other vacant predetermined configuration position having a predetermined

configuration for locating the second semiconductor device thereat; and the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device.

A multi-chip module system comprising: a substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor device thereat, and having at least one other vacant predetermined configuration position for locating a third semiconductor device thereat on the multi-chip module system, the at least one other vacant position having no semiconductor device located thereat; the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; wherein said first and second semiconductor devices being burned in; the at least one other vacant predetermined configuration position for locating the third semiconductor

device thereat which is substantially the same as the predetermined configuration of the first position; the at least one other vacant predetermined configuration position for locating the third semiconductor device thereat; and the third semiconductor device having a third predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device; wherein the first semiconductor device comprises a memory device; wherein the second semiconductor device comprises a memory device; wherein the first semiconductor device comprises a microprocessor device; wherein the second semiconductor device comprises a microprocessor device; wherein the multi-chip module system comprises a single in-line memory module system; an adapter connected to the third semiconductor device, the adapter having a configuration for connecting the adapter to the at least one other vacant predetermined configuration position on the substrate to allow connection of the third semiconductor device to the substrate.

A multi-chip module system comprising: a substrate having two opposing sides, said substrate having a first predetermined configuration position for locating a first semiconductor device thereat, having a second predetermined configuration position for locating a second semiconductor

device thereat, having a first vacant predetermined configuration position for locating a third semiconductor device thereat, the first vacant predetermined configuration position having no semiconductor device located thereat; and having a second vacant predetermined configuration for locating a fourth semiconductor device thereat on the multi-chip module system; the second vacant predetermined configuration position having no semiconductor device located thereat; the first semiconductor device located in the first predetermined configuration position of the substrate for use in the multi-chip module system, the first semiconductor device having a first predetermined performance characteristic; and the second semiconductor device located in the second predetermined configuration position of the substrate for use in the multi-chip module system, the second semiconductor device having a second predetermined performance characteristic; said first and second semiconductor devices have been burned in; the first vacant predetermined configuration position and the second vacant predetermined configuration position are located on opposing sides of the substrate.

To further clarify the disclosure of at least one other vacant position, Corbett discloses that a defective device is removed; therefore, there is a vacant position at the position of the removed device.

Also, although Corbett does not appear to explicitly disclose the process limitations that the devices have been burned in at the positions on the substrate, the burned in devices of Corbett inherently possess any structural characteristics imparted by the process limitation. See In re Fitzgerald, Sanders, and Bagheri, 205 USPQ 594 (CCPA 1980).

To further clarify the disclosure of a second vacant position, Corbett discloses, "The failed parts will then be replaced." Also, Corbett discloses, "If for any reason a failed die 31 becomes defective . . . The defective die 31 can be removed," and, it is well settled that the term "a" or "an" ordinarily means "one or more." Tate Access Floors, Inc., and Tate Access Floors Leasing, Inc., v. Interface Architectural Resources, Inc., 279 F.3d 1357; 2002 U.S. App. LEXIS 1924; 61 U.S.P.Q.2D (BNA) 1647 ((citing Tate Access Floors, Inc. v. Maxcess Techs., Inc, 222 F.3d 958, 966 n.4, 55 U.S.P.Q.2D (BNA) 1513, 1518 [**32] (citing Elkay Mfg. Co. v. Ebco Mfg. Co., 192 F.3d 973, 977, 52 U.S.P.Q.2D (BNA) 1109, 1112 (Fed. Cir. 1999))). Therefore, Corbett discloses a second removed device, and, there is a second vacant position at the position of the second removed device.

Furthermore, it is inherent that the first and second removed devices of Corbett are replaced either simultaneously or sequentially, and these two alternatives can be at once envisaged. In addition, when the first and

second removed devices are replaced simultaneously, there is a first and second vacant position prior to replacement; and, when the second device is removed from a position on the side opposing the first vacant position, there is a second vacant position at the position of the removed second device; and the first vacant position and the second vacant position are on opposing sides of the substrate.

The following claim limitations are statements of intended use:

For locating a first semiconductor device thereat; for locating a second semiconductor device thereat on the multi-chip module system; until a semiconductor device is installed to replace a defective semiconductor device at another position; for use in the multi-chip module system; for locating the second semiconductor device thereat, and the second semiconductor device having a second predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device; for locating a second semiconductor device thereat; for locating a third semiconductor device thereat on the multi-chip module system; for locating a third semiconductor device thereat; for locating a third semiconductor device thereat, and the third semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the

first semiconductor device; wherein the second semiconductor device comprises a memory device; wherein the second semiconductor device comprises a microprocessor device; for connecting the adapter to the at least one other vacant position on the substrate to allow connection of the third semiconductor device to the substrate; for locating a fourth semiconductor device thereat on the multi-chip module system; for locating the second semiconductor device thereat, and the second semiconductor device having a predetermined performance characteristic of at least substantially twice that of the first predetermined performance characteristic of the first semiconductor device; for locating the third semiconductor device thereat; for locating the third semiconductor device thereat, and the third semiconductor device having a third predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device; for connecting the adapter to the at least one other vacant predetermined configuration position on the substrate to allow connection of the third semiconductor device to the substrate.

Although, as elucidated supra, Corbett discloses many of these intended use limitations, Corbett does not appear to explicitly disclose all of them.

Nonetheless, these statements of intended use do not result in a structural difference between the claimed multi-chip module and the multi-chip module of Corbett. For example, in claim 21, the intended use limitation, "for locating the second semiconductor device thereat," does not structurally limit the claimed multi-chip module to a second semiconductor device located thereat. In fact, there cannot be a device located at the vacant position. Hence, the further limitation, "and the second semiconductor device having a predetermined performance characteristic substantially similar to that of the first predetermined performance characteristic of the first semiconductor device," does not further limit the scope of the claims. Further, because the multi-chip module of Corbett has the same structure as the claimed multi-chip module, it is inherently capable of being used for the intended uses, and the statements of intended use do not patentably distinguish the claimed multi-chip module from the multi-chip module of Corbett. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in

determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

Applicant's remarks filed on 1-24-5 have been fully considered adequately addressed in the rejections.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee

pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR: Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
15-Apr-05